REMARKS

Please reconsider the present application in view of the above amendments and the following remarks. Applicant thanks the Examiner for carefully considering the present application and for indicating that claims 17 – 23, 29 – 35, and 41 – 47 contain allowable subject matter.

I. Status of Claims

Claims 1 – 47 were pending in the present application. By way of the Response to the Office Action of March 8, 2005, claim 11 was canceled without prejudice or disclaimer. Accordingly, claims 1 – 10 and 12 – 47 are currently pending in the present application.

II. Amendments to the Claims

Claim 8 has been amended to correct a typographical error. No new matter has been added by way of this amendment.

III. Objections to the Claims

Claim 8 was objected to as containing a typographical error. By way of this reply, claim 8 has been amended to correct this typographical error. Accordingly, withdrawal of the objection to claim 8 is respectfully requested.

IV. Rejections Under 35 U.S.C § 102

Claims 1 – 4, 6, 10, 12, 14 – 16, 24, 26 – 28, 36, and 38 – 40 of the present application were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,680,636 issued to Parry et al. (hereinafter "Parry"). For the reasons set forth below, this

rejection is respectfully traversed.

The present invention is directed to a technique for reducing clock skew using one or more biasable drivers. With reference to Figures 5a – 5d of the present application, a biasable driver (e.g., **104**) is selectively sized depending on a delay of a clock signal from a clock source **17** to a point (e.g., point **y**), where the biasable driver (e.g., **104**) inputs the clock signal at the point (e.g., point **y**). *See* Specification, paragraphs [0033] – [0037]. Accordingly, independent claims 1, 12, 24, and 36 of the present application require, in part, the selective sizing of a biasable driver be dependent on a delay of a clock signal from a clock source to an input of the biasable driver.

Parry, in contrast to the present invention, fails to disclose at least the limitations of the claimed invention discussed above. Parry discloses a clock edge placement circuit that has a delay line that adds propagation delay to a clock signal at an input of the clock edge placement circuit. *See* Parry, Abstract. Figure 6 of Parry shows the structure of the clock edge placement circuit **60**. Delay line **66** has a plurality of taps that may be used to add delay to a clock signal in order to ensure that an edge of the clock signal is placed such it causes optimal sampling by external logic elements. *See* Parry, column 8, lines 20 – 53; Figure 3, reference **39** (showing ideal placement of edge on clock signal **39B** relative to data signal **39A**).

As disclosed in Parry, selecting taps of delay line **66** for adding delay is dependent on a period of the incoming clock signal:

> Referring still to FIG. **6**, determining the correct one of taps **0** through m-1 to select is determined by measuring the period of the incoming clock signal **38***b*. This is accomplished using a "measurement mode" of the clock edge placement circuit **60**. The measurement latch **65** (e.g., the m-bit measurement latch **65**) is used to measure the clock period. The measurement latch **65** includes a series of individual latches (e.g., latch **0** to latch m-1) coupled to the corresponding taps of delay line **66**. During measurement mode, a measurement signal (meas_clk_period) is asserted to the latch controller **63**. This causes latch controller **63** to "open" the latches

> of measurement latch **65** to capture the outputs of the corresponding taps of delay line **66**. The propagation of the start signal along delay line **66** is thus captured by the latches of measurement latch **65**. The output of flip-flop **62** produces an end signal, precisely one clock cycle after the start signal, which causes latch controller **63** to close the latches of measurement latch **65**. This effectively takes a "snap-shot" of the propagation of the start signal along delay line **66**. By examining the contents of the individual latches of measurement latch **65**, the clock period of the incoming clock signal **38***b* can be determined in terms of an integral number of delay elements (e.g., as described in the discussion of FIG. **14** below).
>
> In this manner, the individual latches of measurement latch **65** store the progress of the start signal as it rippled down delay line **66**. Those taps through which the start signal passed have a logical one stored in their respective latches, while those taps not reached by the start signal prior to the end signal have a logical zero stored in their corresponding latches.
>
> The outputs of the individual latches of measurement latch **65** are coupled to edge detector **64**. Edge detector **64** analyzes each of the outputs to determine the progress of the start signal. The number of taps through which the start signal rippled indicates the particular tap output to select in data selector **67**, which, in turn, controls the amount of delay to be added. FIG. **7** graphically depicts this process.

See Parry, column 8, line 54 – column 9, line 24 (emphasis added); *see also, e.g.*, Figures 7 and 8; column 9, line 46 – column 10, line 30; column 16, line 57 – column 17, line 12 ("To implement the first step of clock edge placement, delay stack **313** measures the clock period."). It is clear from the foregoing disclosure in Parry, that delay line **66** adds delay based on a measured period of the incoming clock signal. Those skilled in the art will clearly recognize that a period of a clock signal is the amount of time that elapses during one cycle of the clock signal (period = 1 / frequency). This is distinct from a delay of a clock signal. A signal can be greatly delayed and still have the same clock period it had before the signal was delayed. Conversely, a clock period of a signal may change over time even though the signal itself is not delayed from one point to another. Parry discloses adding delay to an incoming clock signal based on a measured clock period of that signal. Parry clearly fails to disclose, however, sizing a biasable driver *dependent on a delay* of a clock signal *from a clock source to an input of the biasable driver* as required by independent claims 1, 12, 24, and 36 of the present application.

In view of the above, Parry fails to show or suggest the present invention as recited in independent claims 1, 12, 24, and 36 of the present application. Thus, independent claims 1, 12, 24, and 36 are patentable over Parry. Dependent claims are allowable for at least the same reasons. Accordingly, withdrawal of the § 102 rejections is respectfully requested.

V. Rejections Under 35 U.S.C § 103

Claims 5, 7 – 9, 13, 25, and 37 of the present application were rejected under 35 U.S.C. § 103(a) as being unpatentable over Parry. For the reasons set forth below, this rejection is respectfully traversed.

As discussed above, Parry fails to disclose each and every limitation of independent claims 1, 12, 24, and 36 of the present application. Thus, independent claims 1, 12, 24, and 36 are patentable over Parry. Dependent claims 5, 7 – 9, 13, 25, and 37 are allowable for at least the same reasons.[1] Accordingly, withdrawal of the § 103 rejections is respectfully requested.

[1] Moreover, because Parry fails to disclose each and every limitation of independent claims 1, 12, 24, and 36 of the present application, Applicant need not discuss the merits of the Examiner's rejections of those dependent claims also rejected solely under Parry. Thus, Applicant in no way admits to or acquiesces to the various unsupported items of Official Notice taken by the Examiner in paragraphs 19 – 22 of the instant Office Action.

VI. Conclusion

Applicant believes this reply is fully responsive to all outstanding issues and places the present application in condition for allowance. If this belief is incorrect, or other issues arise, the Examiner is encouraged to contact the undersigned or his associates at the telephone number listed below. Please apply any charges not covered, or any credits, to Deposit Account 50-0591 (Reference Number 03226.166001; P7131).

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Respectfully submitted,

By _____

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